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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,729	03/31/2004	Udo Ausserlechner	068758.0195	5141

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EXAMINER	
HOANG, ANN THI	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 01/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/813,729	AUSSERLECHNER, UDO	
	Examiner	Art Unit	
	Ann T. Hoang	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-4, 6-8, 10-11, and 13-14* is/are rejected.

7)☒ Claim(s) *2, 5, 9, 12, and 15-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/31/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: Dn of Fig. 7. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. Figures 7-9 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the

applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities: On page 16, line 2 of paragraph 54, it appears the reference to Fig. 2 is actually referring to Fig. 9. Appropriate correction is required.

Claim Objections

4. Claims 1, 4, 6, 8, 11, and 13 are objected to because the description of the parasitic pn-junction being conductive "*at* a first polarizing potential" or "*at* a second polarizing potential," is unclear. It is suggested that the language of these claims be changed to describe the parasitic pn-junction as being conductive *when* the output is at a first polarizing potential smaller than the first supply potential, or *when* the output is at a second polarizing potential, etc. Appropriate correction is required.

5. Claims 7 and 14 are objected to because there is insufficient antecedent basis for the output OUT. It is recommended that the reference OUT be removed from the claims. Appropriate correction is required.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 3-4, 6-8, 10-11, and 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gariboldi et al. (US 5,182,470) in view of Lee et al. (US 5,270,565).

Regarding claim 1, Gariboldi et al. discloses a semiconductor circuit in a semiconductor substrate (1), comprising: a first input for feeding a first supply potential ($-V_{EE}$); a second input for feeding a second supply potential (V_{CC}) higher than the first supply potential; a device (connected to V_{OUT}); an output (V_{OUT}); a parasitic pn-junction (DP_1) between the device and the semiconductor substrate (1), which is conductive when a first polarizing potential at the output (V_{OUT}) is smaller ($V_{OUT} < -V_{EE}$) than the first supply potential; and a protective circuit (D_1, Q, R_L) connected between the output (V_{OUT}) and the pn-junction (DP_1). The device is an output stage such as a driving stage or line driver for transmitting data. Protective circuit (D_1, Q, R_L) blocks a high current occurring during a negative overvoltage, that is when ($V_{OUT} < -V_{EE}$), that would otherwise compromise the integrity of the stage. See abstract; Figs. 2-3; column 1, lines 67-68; and column 2, lines 1-13. Gariboldi et al. only deals with protection against negative overvoltages and does not disclose protective circuit (D_1, Q, R_L) to have an increased electric resistance when the output is at the first polarizing potential or when it is at a second polarizing potential greater than the second supply potential (V_{CC}), compared to when the output is at a normal operation potential between (V_{CC}) and ($-V_{EE}$).

However, Lee et al. recognizes the need for protection against both positive and negative overvoltages at an output by disclosing an electro-static discharge protection circuit that provides protection to an integrated circuit during ESD events, that is when the output voltage is above the supply potential or below the reference potential. Lee et al. discloses a protective circuit (14, 16, 22) connected to an output (10), whose electric resistance during an ESD event is higher than that during normal operation. The purpose disclosed which the protective circuit (14, 16, 22) serves is to limit the current generated during the ESD event that would otherwise irreversibly damage the circuit. See abstract; Fig. 3; column 4, lines 28-31 and 63-68; column 5, lines 1-10; and column 7, lines 18-32. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the protection circuit of Lee et al. into the semiconductor circuit of Gariboldi et al. in order to provide highly resistive current limiting means during both positive and negative overvoltages, thereby preventing damage to the circuit due to high currents occurring during the overvoltages, while also reducing the resistance of the protection circuitry during normal operation to allow the current to flow more uninhibitedly during normal operation.

Regarding claim 3, the protective circuit (14, 16, 22) of Lee et al. includes a MOSFET (14), the channel of which comprises the same conductivity type as the semiconductor substrate (28). MOSFET (14) and substrate (28) are both p-type. See column 6, line 25 and column 8, lines 39-42.

Regarding claim 4, Gariboldi et al. discloses that semiconductor substrate (1) is a p-doped semiconductor substrate and that the pn-junction (DP_1) is conductive at the

first polarizing potential at the output (V_{OUT}) smaller than the first supply potential ($-V_{EE}$). See Fig. 2; column 1, lines 47-49 and 67-68; and column 2, lines 1-13.

Regarding claim 6, Gariboldi et al. discloses that the parasitic pn-junction (DP_1) is a pn-junction between the semiconductor substrate (1) and a part of the device, which is non-conductive when the potential at the output (V_{OUT}) is greater than the first supply potential ($-V_{EE}$). See column 1, lines 67-68 and column 2, lines 1-13. The pn-junction would also be non-conductive during an output potential smaller than a second supply potential in the combination of Gariboldi et al. and Lee et al. mentioned above, which provides both negative and positive overvoltage protection.

Regarding claim 7, Gariboldi et al. discloses the device as being a digital output stage with the output (V_{OUT}). See column 2, lines 42-47.

Regarding claim 8, Gariboldi et al. discloses a semiconductor circuit in a semiconductor substrate (1), comprising: a first input for feeding a first supply potential ($-V_{EE}$); a second input for feeding a second supply potential (V_{CC}) higher than the first supply potential; an output stage coupled between the first and second input comprising an output (V_{OUT}) and a parasitic pn-junction (DP_1) between the output stage and the semiconductor substrate (1), which is conductive when a first polarizing potential at the output (V_{OUT}) is smaller ($V_{OUT} < -V_{EE}$) than the first supply potential; and a protective circuit (D_1, Q, R_L) connected between the output (V_{OUT}) and the pn-junction (DP_1). See abstract; Figs. 2-3; column 1, lines 67-68; and column 2, lines 1-13 and 42-47. Gariboldi et al. only deals with protection against negative overvoltages and does not disclose protective circuit (D_1, Q, R_L) to have an increased electric resistance when the

output is at the first polarizing potential or when it is at a second polarizing potential greater than the second supply potential (V_{CC}), compared to when the output is at a normal operation potential between (V_{CC}) and ($-V_{EE}$).

However, Lee et al. recognizes the need for protection against both positive and negative overvoltages at an output by disclosing an electro-static discharge protection circuit that provides protection to an integrated circuit during ESD events. Lee et al. discloses a protective circuit (14, 16, 22) connected to an output (10), whose electric resistance during an ESD event is higher than that during normal operation. Protective circuit (14, 16, 22) limits the current generated during the ESD event that would otherwise irreversibly damage the circuit. See abstract; Fig. 3; column 4, lines 28-31 and 63-68; column 5, lines 1-10; and column 7, lines 18-32. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the protection circuit of Lee et al. into the semiconductor circuit of Gariboldi et al. in order to provide highly resistive current limiting means during both positive and negative overvoltages, thereby preventing damage to the circuit due to high currents occurring during the overvoltages, while also reducing the resistance of the protection circuitry during normal operation to allow the current to flow more uninhibitedly during normal operation.

Regarding claim 10, claim 10 corresponds to claim 3 and is rejected under the same reasoning as that of claim 3. See above rejection.

Regarding claim 11, claim 11 corresponds to claim 4 and is rejected under the same reasoning as that of claim 4. See above rejection.

Regarding claim 13, claim 13 corresponds to claim 6 and is rejected under the same reasoning as that of claim 6. See above rejection.

Regarding claim 14, claim 14 corresponds to claim 7 and is rejected under the same reasoning as that of claim 7. See above rejection.

Allowable Subject Matter

8. Claims 2, 5, 9, 12, and 15-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claims 2 and 9, the prior art fails to teach the protective circuit mentioned above to include a JFET.

Regarding claims 5 and 12, the prior art fails to teach the protective circuit mentioned above to have a positive temperature coefficient.

Regarding claims 15-20, the prior art fails to teach the protective circuit mentioned above as being connected in the configuration described in claim 15, wherein a FET is coupled with its drain source path being between the output and the parasitic pn-junction, and with its gate being coupled to the output via a diode.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Walther et al. discloses a switching device with polarity reversal protection. DeShazo et al. discloses an IC with short circuit current protection via a parasitic diode.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ann T. Hoang, whose telephone number is 571-272-2724. The examiner can normally be reached Monday through Friday, 8:00 a.m. to 5:00 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus, can be reached at 571-272-2058. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR: Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ATH
1/17/06

PHUONG T VU
PRIMARY EXAMINER